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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,846	07/10/2003	Amanda C. Caswell	AUS920030426US1	1734

7590 03/06/2006

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EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,846	CASWELL ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 01 July 1003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 20 are presented for the examination.

Specification

2. The disclosure is objected to because of the following informalities:

3. In specification in line 9 on page 7, replace "master control" with ---master controller---as reference numeral 102 is referred to master controller.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1 – 20, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kapur et al. [hereinafter as Kapur], US Patent 6,615,380 B1 and further in view of Saxena et al. [hereinafter as Saxena], US Patent 6, 766, 487 B2.

5. As to claims 1,13, and 19, Kapur discloses a electronics design automation [EDA] system for designing integrated circuits [IC] with design for test [DFT] technique and test synthesis tool and method including computer program product for configuration circuitry for partitioning at least one scan chain into a plurality [multiple] of segments and enables each segment to be selectively bypassed or deactivated during the test application [col. 1, lines 7 – 10, 23 – 40, col. 2, lines 17 – 28, col. 4, lines 26 – 34,].

However, Kapur does not teach explicitly scanning one of the plurality of segments at a time.

Saxena teaches a low power scan architecture [scan circuitry] [col. 1, lines12 – 13] including a processor [core] having one or more scan chains with multiple segments [fig. 20] and method for scanning including scanning one of the plurality of segments at a time [col. 3, lines 35 – 55, col. 4, lines 43 – 67, col. 5, lines 17 – 52, col. 11, lines 47 – 67, col. 12, lines 1 – 30, col. 13, lines 32 – 57, col. 15, lines 9 – 67, col. 16, lines 1 – 46].

It would have been obvious to one of ordinary skill in art, having the teachings of Kapur and Saxena before him at the time of invention was made, to modify the EDA system, DFT technique and a test synthesis tool to include scanning [testing] of each circuit [segment] at a time as taught by Saxena in order to obtain an improved test synthesis tool to provide direct synthesis of low power scan architecture and eliminate the need to perform the adaptation steps [col. 12, lines 25 – 40].

6. As to claims 2, 8, and 14, Kapur teaches an EDA system with DFT and a test synthesis tool with reconfiguration circuitry for partitioning the scan chain into multiple

segments including desired number of partitions with parameterizable which includes predetermined length and an offset segment [col. 2, lines 24 – 26, 50 – 57, col. 9, lines 16 – 24].

7. As to claims 3, 9, and 15, Kapur teaches an EDA system with DFT and a test synthesis tool with reconfiguration circuitry for partitioning the scan chain into multiple segments including desired number of partitions with parameterizable which includes an offset segment to handle variable length between the one or more scan chains [col. 2, lines 24 – 26, 50 – 57, col. 9, lines 16 – 24].

8. As to claims 4, 10, and 16, Saxena teaches scan test operation including scan control sequencing operation including scanning one or more of the plurality of segments one at a time to complete scanning the at least one scan chain [col. 5, lines 46 – 52, col. 13, lines 48 – 57] including enough clocking to scan all bits and keep track of predetermined length [by using counter], and offset segment [col. 19, lines 30 – 67, col. 20, lines 1 – 67, col. 21, lines 1 – 43, fig. 23 – 25].

9. As to claims 5, 11, and 17, Saxena teaches scan test operation including scan control sequencing operation which inherently includes scanning any remaining one or more of the plurality of segments one at a time to complete scanning the at least one scan chain [col. 5, lines 46 – 49].

10. As to claim 20, Kapur teaches EDA systems with with DFT and a test synthesis tool with scan circuitry including reconfiguration circuitry for partitioning the scan chain into multiple segments and an off-chip memory [102 RAM] coupled to master controller [101] for storing unloaded content [fig. 1].

11. **Examiner's note**: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

12. **Prior Art not relied upon**: Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 6:45 am - 5:15 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
February 24, 2006

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
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